A 20mA Quiescent Current CV/CC Parallel Operation HBT Power Amplifier for W-CDMA Terminals

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Abstract — **A novel constant voltage / constant current (CV/CC) parallel operation HBT power amplifier (PA) configuration is proposed. By combining two HBT's having different base bias circuits for each (one is CV and the other is CC), non-linearity at large back-off region can be canceled out. Therefore, both low quiescent current and enough ACPR performance can be achieved. The fabricated CV/CC parallel operation HBT PA demonstrates extremely low quiescent current of 20mA and ACPR of less than -38dBc at the output power range up to 27.5dBm.**

I. Introduction

Low quiescent current and high efficiency at the maximum output power are key issues for PA's used in CDMA terminals including W-CDMA [1]-[4]. In the case of near pinch-off biased HBT PA using a conventional constant voltage base bias circuit, low quiescent current operation is available and high efficiency at maximum output power can be achieved, whereas the adjacent channel power leakage ratio (ACPR) can not satisfy the specification due to the non-linearity in the large back-off region. In even combined configuration of class AB and class C amplifiers which allow lower quiescent current [3], the distortion is worse by rapidly gain increase in class C amplifier. For this reason, collector voltage control system by using DC/DC converter has been also investigated [4]

In this paper, a novel CV/CC parallel operation HBT PA is described. This PA configuration allows us to obtain low quiescent current characteristics without any external control circuits or DC/DC converter. This PA employs parallel connected HBT's having different base bias circuit each other. One is a CV base bias circuit and the other is a CC circuit. Near pinch-off region, a HBT PA employing a CV base bias circuit has positive gain deviation versus output power and that employing a CC base bias circuit has negative gain deviation. By selecting suitable finger number and initial base bias conditions for each CV/CC base drive HBT's, the gain deviation is cancelled out, and adequate linearity can be achieved. The measured results show the effectiveness of this CV/CC parallel operation HBT PA.

II. Configuration Of CV/CC Parallel Operation HBT PA

Figure 1 shows the block diagram of the CV/CC parallel operation HBT PA. The amplifier has two HBT's connected in parallel and both have separated base bias circuits for CV and CC drive. To operate the HBT's on the different bias conditions, two capacitances at base of each HBT are inserted. The HBT's have common emitter and common collector electrode. The two HBT's for PA and the base bias circuits are integrated into a single chip. The matching circuits for both input and output are common, and they are designed with taking into account of the second harmonic frequency component. Vcc bias circuit is also common and Vcc is 3.5V.

A HBT PA employing a CV base bias circuit (upper in Fig.1) has positive gain deviation versus output power near pinch-off region and that employing a CC base bias circuit (lower in Fig.1) has negative gain deviation at the same time. By connecting each CV/CC base drive HBT's in parallel, the gain deviation is cancelled out and the linearity is improved.

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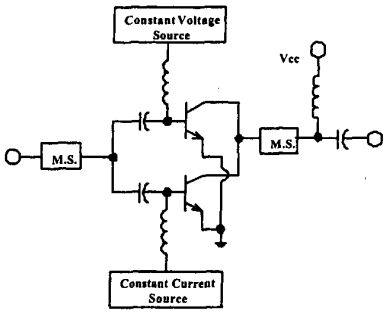
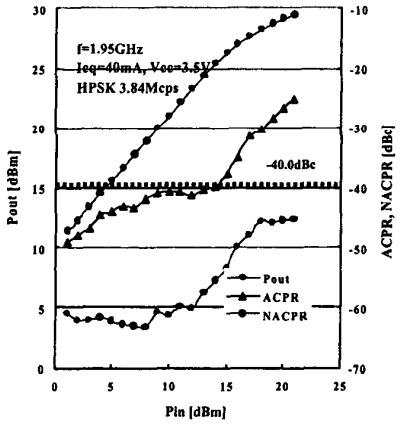


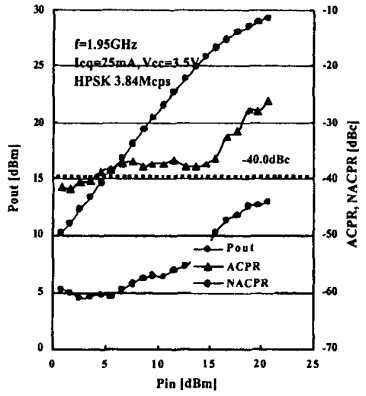
Fig.1 Block diagram of CV/CC parallel operation HBT PA. (M.S. means Matching Section.)

III. Distortion Cancellation by CV/CC Parallel Operation HBT Configuration

At the beginning, the conventional CV operation HBT PA performances are evaluated as the standard. In this evaluation, the constant current source shown in Fig.1 is replaced with the constant voltage source. Fig. 2 shows the measured transfer characteristics of CV operation HBT PA at (a) 40mA and (b) 25mA quiescent current conditions. In the case of 40mA, ACPR does not exceeds -40dBc at Pout < 24.9 dBm, whereas in the case of 25mA, ACPR exceeds -40dBc even in large back-off region. This result indicates the limitation to lower the quiescent current of the conventional CV base drive HBT PA.



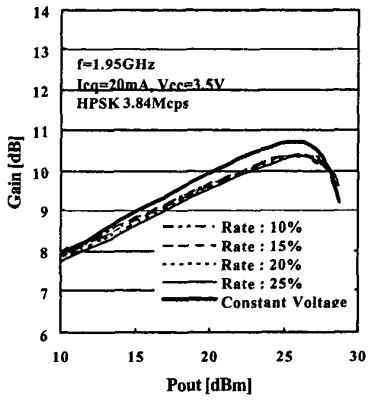
(a) Icq = 40mA



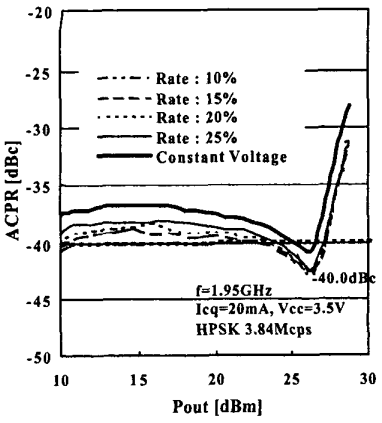
(b) Icq=25mA

Fig.2 Measured transfer characteristic of convent ional CV base biased HBT PA. (Icq : Quiescent current.)

Figure 3 shows the measured output power dependences of gain and ACPR deviation for CV/CC parallel operation HBT PA. The transistor finger number ratio of CV and CC HBTs are 3:1. In this figure, the parameter is the ratio of quiescent current of the CC HBT per total quiescent current. If the bias conditions of each HBT's are same at small signal region, "Rate" becomes 25%. By changing the bias condition of CC HBT to the near pinch-off, gain deviation becomes flat at large back-off region and the ACPR improved. In the case of "Rate" below 10%, ACPR becomes to satisfy the target of -40dBc. Thus, a pair of CV/CC parallel operation HBT's have a capability to cancel out their distortion generated in each others by selecting the optimum transistor sizes and bias conditions at idle state.



(a) Gain deviation



(b) ACPR deviation

Fig.3 Measured output power dependences of gain and ACPR deviation for CV/CC parallel operation HBT PA.

IV. Measured Results of The Fabricated PA

Figure 4 shows a microphotograph of fabricated CV/CC parallel operation PA chip. Die area is 0.8mm x 0.8 mm. It consists of a pair of HBT's and the two different bias circuits for single stage PA. At this time of evaluation, external base bias circuits have been used to optimize the bias condition of each HBT's and internal bias circuits did not be used.

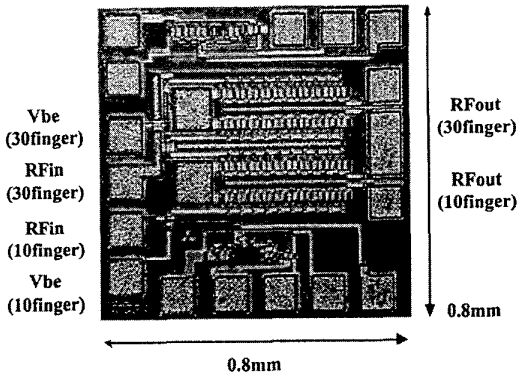
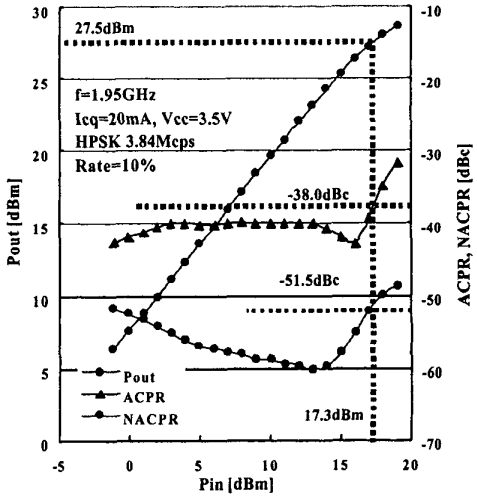


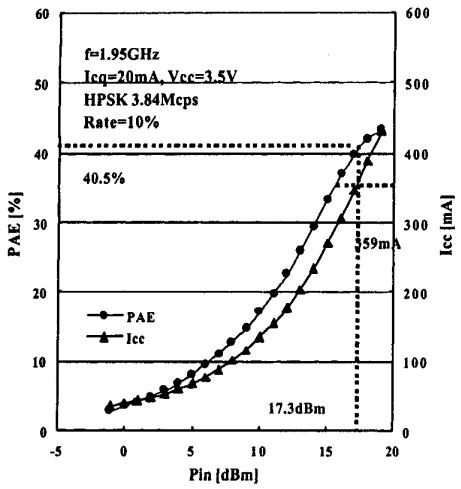
Fig. 4 Microphotograph of fabricated CV/CC parallel operation PA chip.

According to the investigation of "Rate" in quiescent current of each HBT's, "Rate" is designed as 10%. Fig.5(a) shows the measured transfer characteristics of Pout and ACPR and next ACPR (NACPR). Fig.5(b) shows the power added efficiency (PAE) and total current of the PA at the same time. From these figures, very low quiescent current of 20mA is achieved with below -40dBc ACPR at large back-off region. At maximum output power region, Pout of 27.5dBm and PAE of 40.5% are obtained with ACPR of -38dBc and NACPR of -51.5dBc.

Table 1 shows the comparison of measured RF performances between the conventional CV base biased HBT PA and the proposed CV/CC parallel operation HBT PA. Comparing with conventional PA, the proposed PA configuration enables to achieve low quiescent current operation with adequate ACPR performance at low power range and does not degrade the RF performances at maximum output power range.



(a) Pout, ACPR and NACPR versus Pin.



(b) PAE and Icc versus Pin.

Fig.5 Measured transfer characteristics of CV/CC parallel operation PA.

V.CONCLUSION

A novel CV/CC parallel operation HBT PA is described. By combining a pair of CV and CC base biased HBT's, non-linearity of each HBT is cancelled out. Thus, low distortion characteristics (i.e. ACPR) at large back-off region have been achieved. At maximum output region, almost no degradations of Pout and PAE are observed. This novel PA configuration is quite suitable to those PA's used in CDMA (W-CDMA) terminals which have been requested to achieve extremely low quiescent current.

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Table1 Comparison of measured RF performances between the conventional CV base biased HBT PA and the proposed CV/CC parallel operation HBT PA.

Base Bias Condition	Icq [mA]	Icc [mA] @Pout=12dBm	Pout_max [dBm] @ACPR=-38dBc	PAE [%] @ACPR=-38dBc
CV	40	56.4	26.2	33.1
CV/CC	20	38.2	27.5	40.5